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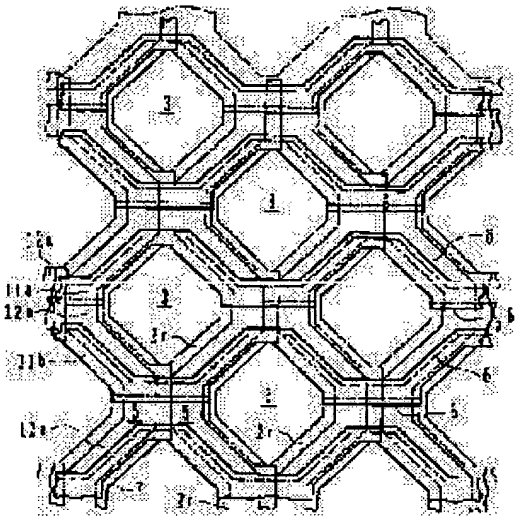
(54) CHARGE TRANSFER PATH AND SOLID STATE IMAGE SENSOR USING IT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a high integration solid state image sensor having high photoelectric conversion function and high transfer function.
SOLUTION: The solid state image sensor comprises multiple photoelectric conversion elements arranged in matrix on the surface of a semiconductor substrate such that the photoelectric conversion elements in the even column are shifted from the odd column by one half pitch in each column while the photoelectric conversion elements in the even row are shifted from the odd row by one half pitch in each row, and a plurality of transfer electrodes having an end part overlapping arrangement defining a plurality of section lines on a transfer channel region extending in the row direction while traversing the transfer channel region and a plurality of channel regions having a stripe plan view formed proximately to a corresponding column of photoelectric conversion elements on the semiconductor substrate and extending in the column direction while snaking. Each transfer channel region includes a region where a plurality of channel transfer sections are juxtaposed.



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CLAIMS

[Claim(s)]
[Claim 1] The charge transfer way characterized by providing the following. The semiconductor substrate which has the surface field of the 1st conductivity type. The channel field which is formed in the aforementioned surface field, has the 2nd conductivity type contrary to the 1st conductivity type of the above, has the band-like flat-surface configuration demarcated by one pair of side edges, and extends as a whole in the one direction (the extension direction) of [in a semiconductor substrate front face]. The insulator layer which covered the aforementioned channel field and was formed on the aforementioned semiconductor substrate. The field two or more aforementioned charge transfer partitions **** along the rectangular direction which crosses the aforementioned channel field upper part, is formed on the aforementioned insulator layer, has the edge superposition composition which demarcates two or more compartment lines on the aforementioned channel field, has two or more transfer electrodes which demarcate two or more charge transfer partitions lined [aforementioned] off in the aforementioned channel field, and intersects perpendicularly in the aforementioned extension direction.
[Claim 2] The charge transfer way according to claim 1 where the configuration of the aforementioned channel field and two or more aforementioned transfer electrodes is chosen so that the at least 1 section of the aforementioned compartment line may form the angle of 5 times or more to the aforementioned rectangular direction.
[Claim 3] The charge transfer way according to claim 1 or 2 where the at least 1 section of the aforementioned compartment line has a portion almost parallel to the aforementioned side edge.
[Claim 4] The charge transfer way according to claim 1 or 2 which has the portion to which the at least 1 section of the aforementioned charge transfer partition changes the width of face of the aforementioned rectangular direction in monotone.
[Claim 5] A charge transfer way given in the claim 1 which has the portion toward which the at least 1 section of the aforementioned compartment line inclined 5 times or more to the aforementioned rectangular direction in the field in which the aforementioned channel field extended in the aforementioned extension direction, lying in a zigzag line periodically, and inclined to the aforementioned extension direction, or any 1 term of 4.
[Claim 6] The charge transfer way according to claim 5 with which the adjoining aforementioned charge transfer partition is in contact through the straight-line-like compartment line in the field which inclined to the aforementioned extension direction.
[Claim 7] A charge transfer way given in the claim 1 in which the at least 1 section of two or more aforementioned charge transfer partitions has a narrow portion and a broad portion about the width of face of the aforementioned rectangular direction, or any 1 term of 3.
[Claim 8] The charge transfer way according to claim 7 which has the aforementioned broad portion in one edge of a charge transfer partition.
[Claim 9] The charge transfer way according to claim 8 where the adjoining aforementioned charge transfer partition has the aforementioned broad portion in both the meeting portions.
[Claim 10] A charge transfer way given in the claim 7 which is decreasing the width of face of the aforementioned rectangular direction as the aforementioned narrow portion separates from the aforementioned broad portion, or any 1 term of 9.

[Claim 11] Many optoelectric transducers arranged by two or more trains and the multi-line in the pitch fixed on the front face of the semiconductor substrate which is characterized by providing the following, and which demarcates (a) two-dimensional front face, and the (b) aforementioned semiconductor substrate. the optoelectric transducer of an odd number train — receiving — the optoelectric transducer of an even number train — about 1 of optoelectric-transducer pitch within each train/2 — shifting — **** — the optoelectric transducer of odd lines — receiving — the optoelectric transducer of even lines — about [of the optoelectric-transducer pitch in each line] — many optoelectric transducers in which it is shifted 1/2 and each aforementioned optoelectric-transducer train contains only the optoelectric transducer of an odd number train or an even number train (c) Two or more transfer channel fields which each approaches a corresponding optoelectric-transducer train, are formed on a semiconductor substrate, have the band-like flat-surface configuration demarcated by one pair of side edges, and extend in the direction of a train, moving in a zigzag direction. (d) They are two or more transfer electrodes which cross the aforementioned transfer channel field upper part, and extend in a line writing direction as a whole. It has the edge superposition composition which demarcates two or more compartment lines on the aforementioned transfer channel field, and has two or more transfer electrodes which demarcate two or more charge transfer partitions lined [aforementioned] off in each aforementioned transfer channel field. in each aforementioned transfer channel field The field where two or more aforementioned charge transfer partitions coexist along with the aforementioned line writing direction.
[Claim 12] The solid state camera according to claim 11 as which the configuration of the aforementioned channel field and two or more aforementioned transfer electrodes is chosen so that the at least 1 section of the aforementioned compartment line may form the angle of 5 times or more to the aforementioned line writing direction.
[Claim 13] The solid state camera according to claim 11 or 12 in which the at least 1 section of the aforementioned compartment line has a portion almost parallel to the aforementioned side edge.
[Claim 14] The solid state camera according to claim 11 or 12 which has the portion to which the at least 1 section of the aforementioned charge transfer partition changes the width of face of the aforementioned line writing direction in monotone.
[Claim 15] A solid state camera given in the claim 11 which has the portion toward which the at least 1 section of the aforementioned compartment line inclined 5 times or more to the aforementioned line writing direction in the field in which the aforementioned transfer channel field extended in the aforementioned train direction, lying in a zigzag line periodically, and inclined to the aforementioned train direction, or any 1 term of 14.
[Claim 16] The solid state camera according to claim 15 with which the adjoining aforementioned charge transfer partition is in contact through the straight-line-like compartment line in the field which inclined to the aforementioned line writing direction.
[Claim 17] A solid state camera given in the claim 11 in which the at least 1 section of two or more aforementioned charge transfer partitions has a narrow portion and a broad portion about the width of face of the aforementioned line writing direction, or any 1 term of 13.
[Claim 18] The solid state camera according to claim 17 which has the aforementioned broad portion in one edge of a charge transfer partition.
[Claim 19] The solid state camera according to claim 18 in which the adjoining aforementioned charge transfer partition has the aforementioned broad portion in both the meeting portions.
[Claim 20] A solid state camera given in the claim 17 which is decreasing the width of face of the aforementioned line writing direction as the aforementioned narrow portion separates from the aforementioned broad portion, or any 1 term of 19.
[Claim 21] Two ratios with two or more aforementioned arbitrary charge transfer partitions are solid state cameras given in any 1 term of the claims 11-20 from 1:1 to 1:5.
[Claim 22] Many optoelectric transducers arranged by two or more trains and the multi-line in the pitch fixed on the front face of the semiconductor substrate which is characterized by providing the following, and which demarcates a two-dimensional front face, and the aforementioned semiconductor substrate. the optoelectric transducer of an odd number train —

receiving — the optoelectric transducer of an even number train — about 1 of optoelectric-transducer pitch within each train/2 — shifting — **** — the optoelectric transducer of odd lines — receiving — the optoelectric transducer of even lines — about [of the optoelectric-transducer pitch in each line] — many optoelectric transducers in which it is shifted 1/2 and each aforementioned optoelectric-transducer train contains only the optoelectric transducer of an odd number train or an even number train Two or more transfer channel fields which each approaches a corresponding optoelectric-transducer train, are formed on a semiconductor substrate, have the band-like flat-surface configuration demarcated by one pair of side edges, and extend in the direction of a train, moving in a zigzag direction. They are two or more transfer electrodes which cross the aforementioned transfer channel field upper part, and extend in a line writing direction as a whole. It has the edge superposition composition which demarcates two or more compartment lines on the aforementioned transfer channel field. In the position which has two or more transfer electrodes which demarcate two or more charge transfer partitions lined [aforementioned] off in each aforementioned transfer channel field, and approached the aforementioned optoelectric transducer in each aforementioned transfer channel field The process which is the drive method of driving the solid state camera which includes the field where two or more aforementioned charge transfer partitions coexist along with the aforementioned line writing direction, and accumulates a charge to the (a) aforementioned optoelectric transducer. (b) The process which impresses the high-level voltage for a transfer to the 2nd charge transfer partition which adjoins the line writing direction while reading to the 1st charge transfer partition which adjoins the aforementioned optoelectric transducer and impressing the voltage of level, and the process which changes the voltage of the 1st charge transfer partition of (c) above to the high level for a transfer.

[Claim 23] The drive method of a solid state camera according to claim 22 that the aforementioned process (b) and (c) are repeatedly performed to the optoelectric transducer of odd lines, and the optoelectric transducer of even lines.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the solid state camera using a charge transfer way, the charge transfer way which has improved especially the transfer performance about the solid state camera which used it, and it.
[0002] In addition, in this specification, a transfer performance shows the concept containing a transfer rate and a transfer efficiency.
[0003]
[Description of the Prior Art] A charge transfer way can be formed by forming in the semiconductor-region front face of the 1st conductivity type the transfer channel field where the 2nd conductivity type extends, and forming two or more transfer electrodes in this transfer channel field front face through an insulator layer. Capacity coupling of the transfer electrode can be carried out to a transfer channel field, and it can control the potential of a transfer channel field by controlling the voltage. In order to transmit a charge continuously, on a transfer channel field front face, each edge of two or more transfer electrodes is made to overlap, and it forms.
[0004] The solid state camera is known as a semiconductor device using such a charge transfer way. A solid state camera has the charge transfer way formed all over the light-receiving field by approaching each optoelectric-transducer train with the optoelectric transducer arranged in the shape of a matrix. The charge showing pixel information can be taken out outside by reading the charge accumulated at the optoelectric transducer to a charge transfer way, and transmitting a charge transfer way.
[0005] Usually, arrange an optoelectric transducer in the shape of a square matrix, a charge transfer way is made to approach an optoelectric-transducer train, and it forms in the direction of a train in the shape of a straight line. The transfer electrode which controls the potential of a charge transfer way extends in a line writing direction, and has the configuration cut and lacked on each optoelectric transducer.
[0006] Japanese Patent Application No. No. 288856 [eight to] has proposed the solid state camera which adopted pixel staggering of about 1/2 pitch as the direction of a train, and the line writing direction. The optoelectric transducer which is a pixel within each train is arranged in a fixed pitch, and the optoelectric transducer is arranged in the fixed pitch in each line.
[0007] The optoelectric transducer of an even number train is arranged to the optoelectric transducer of an odd number train in the position where the pitch within a train shifted about 1-/2. Moreover, the optoelectric transducer of even lines is arranged to the optoelectric transducer of odd lines in the position where the pitch in a line shifted about 1-/2.
[0008] The composition of this solid state camera is roughly shown in drawing 11 . Many pixels (optoelectric transducer) PIX are arranged in the shape of a matrix, are arranged in Pitch process variable in the direction of a train, and are arranged in Pitch PH at the line writing direction. The optoelectric transducer of the adjoining train is arranged in the direction of a train at abbreviation (1/2) process-variable gap ******, and the optoelectric transducer of an adjoining line is arranged at abbreviation (1/2) PH gap ****** at the line writing direction.

[0009] In addition, a color filter is formed on each pixel PIX, and the color solid state camera is constituted. G (green), B (blue), and R (red) show the color of each pixel. The channel stop field CS enclosing one side side of Pixel PIX, it has been extended and arranged in the direction of a train, and each train is separated electrically. A perpendicular charge transfer channel is formed in the channel stop field CS and the field inserted into Pixel PIX.
[0010] With the 1st polysilicon contest film formed in a semiconductor substrate front face through a silicon-oxide film, and the 2nd polysilicon contest film, the charge transfer electrodes E1 and E2 which extend in the longitudinal direction in drawing are formed. The 1st polysilicon contest film front face is also being worn by the silicon-oxide film, and is insulated from the 2nd polysilicon contest film.
[0011] The charge transfer electrode is formed each two ends of a road. In addition, it sets in the composition of illustration, and since the pixel PIX within each train is formed one 2 end of a road, four transfer electrodes per pixel are formed in each train. By driving four phases of four electrodes per these pixels, the charge read from each pixel can be perpendicularly transmitted independently.
[0012] A charge transfer electrode makes the charge in a charge transfer way transmit in the direction of a train, and two or more electrodes which have an edge in alignment with the line writing direction overlap in the direction of a train, and it is arranged. In pixel staggering arrangement, it is possible to make the position of the adjoining pixel overlap in a line writing direction and the direction of a train. Moreover, it is also easy to obtain two or more sexual desire news in the same position by interpolating the adjoining pixel information. For this reason, it is arrangement effective in acquiring the picture of high pixel density.
[0013] However, if the area of each pixel is expanded, a transfer way will serve as a configuration which moves in a zigzag direction inevitably. When a transfer way winds, compared with a linear transfer way, the transfer distance of a charge becomes long. According to increase of transfer distance, the transfer time also tends to become long.
[0014]
[Problem(s) to be Solved by the Invention] The purpose of this invention is offering the charge transfer way which can improve a transfer performance.
[0015] In the solid state camera which has pixel staggering arrangement, other purposes of this invention are offering the solid state camera which can maintain the function of an optoelectric transducer and can improve the transfer performance of a transfer way while enabling high integration of a pixel.
[0016] The purpose of further others of this invention is offering the efficient drive method of the solid state camera which has pixel staggering arrangement.
[0017]
[Embodiments of the Invention] Drawing 1 -5 show the solid state camera by the 1st example of this invention. Drawing 1 shows the plan of the semiconductor substrate in which even the transfer electrode was formed. The diagram showing the example of arrangement on the front face of a substrate in the state where drawing 2 (A) formed the impurity addition field in the semiconductor substrate, and drawing 2 (B) are the outline cross sections showing the cross-section composition which meets the IIB-IIB line of drawing 2 (A). The outline diagram showing arrangement of the two-layer polysilicon contest electrode which forms drawing 3 (A) in a substrate front face, drawing 3 (B), and (C) are the cross sections showing roughly the cross-section composition of the semiconductor substrate in alignment with the IIIB-IIIB line and IIIC-IIIC in drawing 3 (A).
[0018] As shown in drawing 1 (A), n type field 3 which turns into a charge-storage field of an optoelectric transducer in semiconductor chip front faces, such as silicon, is arranged in the shape of a matrix. In the composition of drawing, in an odd number train and an even number train, the pitch within a train shifts about 1-/2, and n type field 3 is arranged, and also in odd lines and even lines, the pitch in a line shifts about 1-/2, and it is arranged.
[0019] As shown in drawing 2 (A), it is formed in the configuration to which p+ type field 7 extends in the direction of a train in the left-hand side of each train, and the left-hand side of the each n type field 3 is surrounded. p+ type field 7 separates each train electrically. n type

field 5 is moved in a zigzag direction and formed in the direction of a train so that between adjoining p+ type fields 7 and between p+ type field 7 and n type fields 3 of the left-hand side may be sewn. Between this n type field 5 and n type field 3, p- type field 2 is exposed, reads, and it constitutes the gate field.

[0020] p type with which p- type field 2 was formed in n type silicon substrate 1 as shown in drawing 2 (B) -- it forms by the well -- having -- this p type -- n type fields 3 and 5 and p+ type field 7 are formed into the well 2 n type field 3 constitutes the charge-storage field of the photo diode which forms the optoelectric transducer which is a pixel. In addition, a charge-storage field may be called optoelectric transducer. n type field 5 constitutes the perpendicular transfer channel which transmits a charge in the direction of a train. Each impurity addition field is formed of annealing of an ion implantation and after that.

[0021] Laminating transfer electrodes, such as contest polysilicon, are formed through insulator layers, such as a silicon oxide by thermal oxidation, on the semiconductor substrate front face which has composition as shown in drawing 2 .

[0022] Drawing 3 (A) is the plan showing the configuration of a transfer electrode. Drawing 3 (B) and (C) are cross sections which meet the IIIB-IIIB line and IIIC-IIIC line in drawing 3 (A).

[0023] The thermal oxidation film 8 is formed in a semiconductor substrate front face, and the 1st layer polysilicon contest layer is formed on it. By etching, patterning of the 1st layer polysilicon contest layer is carried out to phot lithography, and the 1st polysilicon contest transfer electrodes 11a and 11b are formed. The 1st polysilicon contest transfer electrodes 11a and 11b have a pattern as shown in drawing 3 (A), and they are arranged so that n type field 3 bottom which is a charge-storage field may be surrounded.

[0024] After forming the 1st polysilicon contest transfer electrodes 11a and 11b, the oxide film 9 by thermal oxidation is formed in the front face. After forming the thermal oxidation film 9, the 2nd polysilicon contest layer is formed on a substrate front face, patterning is carried out by phot lithography and etching, and the 2nd polysilicon contest transfer electrodes 12a and 12b are formed of them. The 2nd polysilicon contest transfer electrode encloses n type field 3 bottom, and has the configuration shown by the drawing 3 (A) middle point line.

[0025] As shown in drawing 3 (B) and (C), the 1st polysilicon contest transfer electrode 11 (11a and 11b are named generically by 11) and the 2nd polysilicon contest transfer electrode 12 (12a and 12b are named generically by 12) have the overlap structure which piled up the edge as shown in drawing 3 (B) and (C).

[0026] If the laminating transfer electrode shown by drawing 3 (A) is formed on the substrate shown in drawing 2 (A), it will become the composition shown in drawing 1 .

[0027] In addition, as shown in drawing 3 (B) and (C), after forming the laminating transfer electrodes 11 and 12, the insulating layer 14 which has a flat front face is formed on it. An insulating layer 14 is formed by the laminated structure of the insulating layer which has for example, a silicon-oxide system insulating layer and a flattening function. The light-filter layer 15 is formed on an insulating layer 14.

[0028] The light-filter layer 15 covers the charge-storage field 3 in each pixel, and carries out incidence only of the light of desired wavelength to each pixel. In addition, on the light-filter layer 15, the flattening insulating layer which has a flattening function further is formed, and the shading film which has opening on a charge-storage field is formed on it. On a shading film, the flattening film which has a flattening function further is formed, and a micro lens is formed on it. About the general structure of a solid state camera, the column of the example of JP,61-25224,A can be referred to, for example.

[0029] As shown in drawing 1 , the transfer channel field 5 in which the laminating transfer electrode was formed on it is divided into two or more partitions by the transfer electrode. These partitions are demarcated by the boundary line 6 of the transfer electrode 11 of the 1st layer.

[0030] Drawing 4 (A) is the outline plan showing each partition in the transfer channel field 5. The transfer channel field 5 is divided into partitions S1, S2, and S3 and S4 by the transfer electrodes 11 and 12 of the 1st layer and the 2nd layer formed in the upper part. These four partitions S1 - S4 are repeatedly arranged in the direction of a train.

[0031] The 2nd polysilicon contest electrode 12 is arranged on the partition S1. The 1st polysilicon contest electrode 11 is arranged on the partition S2. On a partition S3 and S4, the 2nd polysilicon contest electrode 12 and the 1st polysilicon contest electrode 11 are arranged similarly. In addition, the transfer way of an odd number train and the transfer way of an even number train have the configuration where the direction pitch of a train shifted about 1-/2.
[0032] In the arrangement shown in drawing 4 (A), each partition has the narrow section with narrow width of face, and the latus broad section of width of face. The adjoining partitions S1 and S2 have touched through boundary layer 6a which has the short horizontal side connected with the shape oblique side of a long straight line to the ends.
[0033] This oblique side is arranged at the side edge of a transfer channel field, and parallel, and a transfer channel field is divided into the two narrow sections located in a line with the line writing direction. Each narrow section has constant width. The field of constant width has the uniform narrow channel effect. In addition, if an oblique side does not need to be strictly parallel to the side edge of a transfer channel field and is substantially parallel, it is good. The broad section is following the both sides of the coexisting narrow section, respectively.
[0034] Each broad section of partitions S2 and S3 has touched through horizontal boundary layer 6b. The broad section has little influence of the narrow channel effect, and it has low potential.
[0035] Drawing 4 (B) is a cross section for explaining the narrow channel effect roughly. n type field 18 is formed all over p- type field 17. With the fixture potential and applied voltage between the p-field 17 and n type field 18, a depletion layer progresses on the outskirts of pn junction of a between [both]. A dashed line 19 shows the one equipotential surface in such a state roughly. When the width of face of n type field 18 is narrow, the depletion layer which develops from both sides will touch, and the potential of the pars basilaris ossis occipitalis of a staging area will also be raised. It not only reduces the equipotential surface 19 crosswise, but it reduces the depth direction. Thus, in a semiconductor region with narrow width of face, potential rises by the narrow channel effect.
[0036] If the width of face of a charge transfer way becomes narrow, it will become difficult to avoid the narrow channel effect. When the width of face of a charge transfer way changes, it may become difficult for potential distribution to arise and to transmit a charge smoothly in a charge transfer way. A charge transfer way is set as the conditions which n type field depletion-izes completely only for example, with fixture potential.
[0037] On the charge transfer way 5 shown in drawing 4 (A), each partition has the broad section with wide width of face, and the narrow section with narrow width of face. Since the width of face of the narrow section is fixed, the narrow channel effect of the narrow section is uniform. the rate in which the broad section with wide width of face receives the narrow channel effect compared with the narrow section with narrow width of face — few — the potential of a broad portion -- the narrow section — although -- it becomes low Therefore, a charge is accumulated with the priority [portion / narrow] to a broad portion.
[0038] When transmitting a charge to a partition S1 from a partition S4, the charge in a partition S4 is distributed with the priority to a broad portion. If the potential of a partition S1 is lowered, the charge accumulated at the broad portion of a partition S4 will be promptly transmitted to the broad portion of a partition S1. For this reason, the transfer performance which transmits a charge to a partition S1 from a partition S4 can be improved.
[0039] The partition S1 and the partition S2 have touched by long boundary layer 6a. If the potential of a partition S2 is lowered when transmitting a charge to a partition S2 from a partition S1, long boundary layer 6a will be crossed and a charge will be transmitted. That is, it is not generated in the length direction of the charge transfer way 5, but the charge transfer which crosses boundary layer 6a is produced so that long boundary layer 6a may be crossed. Since the cross section of a transfer field is large, the transfer performance of the charge transfer through boundary layer 6a improves.
[0040] Thus, although the charge transfer way which has the laminating transfer electrode structure shown in drawing 1 has a meandering configuration, realizing a high transfer performance is expected. When the transfer performance was actually measured, the good

transfer performance was able to be checked.
[0041] Drawing 5 shows the continuation of a drive circuit to a transfer electrode. The case where 4 phase drive circuits are used as a drive circuit is shown. The 1st phase drive power supply phi 1 is connected to 2nd-layer transfer electrode 12a, and the 2nd phase drive power supply phi 2 is connected to it at 1st-layer transfer electrode 11a. Similarly, the 3rd phase drive power supply phi 3 and the 4th phase drive power supply phi 4 are connected to 2nd-layer transfer electrode 12b and 1st-layer transfer electrode 11b.
[0042] Drawing 6 is a timing chart which shows the signal wave form for explaining the drive method of the solid state image pickup device which used 4 phase driving signal. A driving signal has the read-out level R still higher than the high level H for a transfer, a low level L for a transfer, and the high level for a transfer. It is +15V and the read-out level R can read a charge from a charge-storage field to the charge transfer way 5 which adjoins through p- type field 2. The high level H for a transfer is for example, grounding potential, and a low level L for a transfer is -8V.
[0043] The case where read to the 2nd-layer transfer electrode 12, and the signal of level is impressed hereafter is explained. The portion arranged under the layer [inner / the 2nd layer] transfer electrode 12 of p- type field 2 reads, and it is set to gate field 2r (refer to drawing 1 and drawing 2).
[0044] being high-level first in the 1st phase driving signal phi 1 and the 2nd phase driving signal phi 2, as shown in drawing 6 -- carrying out -- the [the 3rd and] -- 4 phase driving signals phi3 and phi4 are maintained to a low level The 1st phase driving signal phi 1 is read, and it is made to go up to level R in this state. A stored charge is read to the charge transfer way 5 which adjoins from the charge-storage fields 3a and 3c of drawing 5 by impression of the read-out level R. Then, the 1st phase driving signal is returned to the high level for a transfer.
[0045] The read charge is distributed under high-level 2nd-layer transfer electrode 12a and 1st phase transfer electrode 11a. Since it uses full [of a transfer channel field] for a charge storage, the transfer performance at the time of read-out can be made high. In addition, it is directly good also as read-out level without the high level for a transfer in the 1st phase driving signal.
[0046] In this state, the charge accumulated, for example to the charge-storage fields 3b and 3d of drawing 5 is in the state which was not yet read to a charge transfer way, but stopped at the charge-storage field. In this state, it is in the state where the charge was read to the half of the charge transfer way 5, and the charge is not read to the charge transfer way of the remaining half. In order to read a charge to all transfer ways, it is necessary to read a charge also from optoelectric transducers 3b and 3d.
[0047] the [next, / the 1st phase and] -- 2 phase driving signals phi1 and phi2 -- a low level -- carrying out -- the [the 3rd phase and] -- 4 phase driving signals phi3 and phi4 -- the object for a transfer -- suppose that it is high-level The 3rd phase driving signal phi 3 is read, and level R is increased. It is read to the charge transfer way 5 where the charge accumulated by impression of this read-out level to the charge-storage fields 3b and 3d in drawing 5 adjoins.
[0048] In this state, the read charge can be transmitted in the direction of a train by driving four phases of transfer electrodes.
[0049] It can replace with the drive circuit of drawing 5 , and 8 phase drive circuits can also be connected to a transfer electrode. A transfer rate can be raised, if a charge is read from the half of a charge-storage field and 8 phase drives are performed.
[0050] Drawing 7 shows the modification of the 1st example. In this composition, it arranges so that compartment-line 6b of the portion which an adjoining charge transfer way touches through a channel stop field may also incline to a line writing direction. By arranging aslant, the length of boundary layer 6b becomes long. That is, since the cross section of the field through which a charge passes becomes large when performing the charge transfer to the partition from a partition, a transfer performance can be raised.
[0051] Drawing 8 (A) shows the solid state camera by the 2nd example of this invention. An optoelectric transducer is arranged in the shape of a matrix by pixel staggering arrangement, a charge transfer way and a channel stop field are arranged in the direction of a train, and the

transfer electrode is arranged at the line writing direction.
[0052] Although boundary layer 6b of the portion which an adjoining charge transfer way counters through a channel stop field is the same as that of the boundary line in the 1st example, unlike the 1st example, boundary layer 6a in the portion pinched between the charge-storage fields where one charge transfer way adjoins in the direction of slant is arranged in the shape of a straight line.
[0053] The point that the point that each partition has a broad portion and a narrow portion, and boundary layer 6a incline from a line writing direction, and are arranged for a long time in the inside of a charge transfer way is the same as the 1st example. By forming boundary layer 6a in the shape of a straight line, the channel width of a narrow portion changes continuously. Even if the narrow channel effect arises, a potential change is monotonous and continuous and possibility of making a charge piling up all over a charge transfer way decreases by suitable voltage impression. Thus, a transfer performance can be raised.
[0054] In addition, where a low level and high-level voltage are impressed to an adjoining partition, the potential of the partition which impressed high-level voltage falls, long boundary layer 6a is crossed, and a highly efficient charge transfer is performed. About the charge transfer which crosses boundary layer 6b, it is the same as that of the 1st example.
[0055] Drawing 8 (B) shows the modification of the 2nd example. By changing the configuration of the 1st-layer transfer electrode 11 and the 2nd-layer transfer electrode 12, it is formed so that boundary layer 6b may also incline horizontally. Boundary layer 6b inclines, the length is long and a charge transfer performance improves by the bird clapper.
[0056] Drawing 9 shows roughly the planar structure of the solid state camera by the 3rd example. In this example, the portion which adjoins read-out gate 2r of the 1st-layer transfer electrodes 11a and 11b cuts and lacks, and the 2nd-layer transfer electrodes 12a and 12b are also changed according to the configuration. In the portion which adjoins read-out gate 2r, when the 2nd-layer transfer electrode 12 has the configuration of a point breadth, the transfer performance in read-out operation can be improved. That is. when reading a charge to the charge transfer way 5 which reads from the charge-storage field 3 and adjoins exceeding gate 2r, the width of face of the field where a charge moves according to the direction of a charge transfer becomes large. For this reason, an efficient charge transfer is expected.
[0057] Drawing 9 (B) shows the modification of the 3rd example.
[0058] the composition of drawing 9 (A) — setting — the transfer electrodes 11 and 12 — right and left — it has an unsymmetrical configuration Since the configurations of a transfer electrode differ by the adjoining channel when impressing a driving signal to a transfer electrode and transmitting a charge all over a transfer way, a transfer performance may be affected.
[0059] The configuration of the transfer electrodes 11 and 12 is changed into the bilateral-symmetry-configuration in the structure of drawing 9 (B). For this reason, when carrying out the charge transfer of the inside of a charge transfer way, the transfer performance of the charge transfer way between each ** can be equalized.
[0060] A solid state camera has pixel staggering structure above, and although the case where a charge transfer way wound was explained, the same structure is employable also to the charge transfer way which extends in the shape of a straight line. Moreover, although the example of a solid state camera was explained, an above-mentioned charge transfer way can be used for a charge transfer way not only a solid state camera but widely.
[0061] Drawing 10 shows the example of the partition configuration in the example of a straight-line-like charge transfer way.
[0062] Drawing 10 (A) shows the case where the straight-line-like charge transfer way 5 is formed of the repeat of four partitions S1, S2, and S3 and S4. Each partition S1 - S4 have a broad portion and a narrow portion like the partition S1 shown in drawing 4 (A) - S4. It is the same as that of a charge transfer of drawing 4 (A) that the efficiency charge transfer through the charge-storage function and long boundary layer 6a by the broad portion can be performed by such composition.
[0063] Drawing 10 (B) is the structure which leaned aslant the horizontal portion of the boundary lines 6a and 6b in the composition of drawing 10 (A). Other portions are the same as that of

drawing 10 (A). By having leaned boundary layer 6b aslant, the length becomes long and a transfer performance improves. Although the boundary line leans to the side edge of a charge transfer way, it is generated in the rectangular direction to a boundary line, and a transfer efficient as mentioned above is possible for a charge transfer.
[0064] Drawing 10 (C) shows the case where the partition S of the same configuration is constituted, by lining [of the shape of a straight line arranged aslant uniformly / 6] off the charge transfer way 5. When a boundary line 6 inclines horizontally, the length becomes long and a transfer performance improves.
[0065] Drawing 10 (D) shows the case where a boundary line 6 is made into a upward chevron pattern. The length of a boundary line 6 becomes long and the transfer performance during an adjoining partition improves.
[0066] In addition, when leaning a boundary line to a horizontal direction or a line writing direction, in order to clarify the leaned effect, as for the angle, considering as 5 times or more is desirable. Although the case where the partition in a charge transfer way had the same area mostly was explained, the area of a partition may not necessarily be fixed. However, as for the not much big difference in the area of each partition, not attaching is desirable in order to perform an efficient charge transfer. For example, the ratio of the area of two partitions has the desirable things arbitrary [in the same charge transfer way] to consider as within the limits of 1:1 to 1:5 (or 5:1).
[0067] Although the case of a two-layer transfer electrode was explained, a charge transfer way can also consist of transfer electrodes of three or more layers. Moreover, a drive method is not restricted to 4 phase drives.
[0068] Although this invention was explained in accordance with the example above, this invention is not restricted to these. for example, various change, improvement, and combination are possible -- this contractor -- obvious -- it will be .
[0069]
[Effect of the Invention] As explained above, according to this invention, the transfer performance of a charge transfer way can be improved.
[0070] By realizing the transfer performance in which the case of the winding charge transfer way is also high, the transfer performance which is not inferior to a straight-line-like charge transfer way is realizable.
[0071] In the solid state camera which has pixel staggering arrangement, although to make a charge transfer way wind is desired, the trouble by making a charge transfer way wind is solvable.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the outline plan showing the 1st example of this invention.
[Drawing 2] It is the diagram and substrate cross section showing roughly the flat-surface configuration of the impurity addition field in the substrate in the 1st example.
[Drawing 3] They are the plan showing the configuration of the two-layer transfer electrode in the 1st example, and the cross section of a substrate perpendicular direction.
[Drawing 4] It is an outline cross section for explaining the diagram and the narrow channel effect which show the partition configuration of the charge transfer channel in the 1st example.
[Drawing 5] It is the outline plan showing connection of the drive circuit in the 1st example.
[Drawing 6] It is the timing chart which shows roughly the drive method of the solid state camera by the 1st example.
[Drawing 7] It is the plan showing the modification of the 1st example.
[Drawing 8] It is the plan showing roughly the composition of the solid state camera by the 2nd example of this invention.
[Drawing 9] It is the plan showing roughly the composition of the solid state camera by the 3rd example of this invention.
[Drawing 10] It is the outline plan showing the charge transfer way by other examples of this invention.
[Drawing 11] It is the plan showing roughly the composition of the solid state camera by the proposal of this invention person's point.
[Description of Notations]
1 N-type-Semiconductor Substrate
2 It is Well P Molds.
3 Five n type field
6 Boundary Line
7 P+ Type Channel Stop Field
8 Nine Silicon-oxide film
11 12 Polysilicon contest transfer electrode
14 Insulating Layer
15 Light-Filter Layer

[Translation done.]

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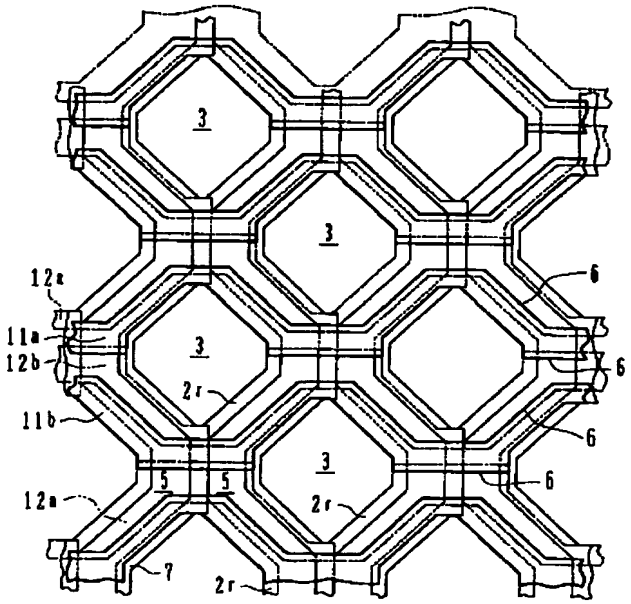
最終頁に続く

(54)【発明の名称】　電荷転送路およびそれを用いた固体撮像装置

(57)【要約】
【課題】　高集積度，高光電変換機能，高転送性能の固体撮像素子を提供する。
【解決手段】　半導体基板の表面に行列状に配列され、奇数列に対し、偶数列の光電変換素子は各列内のピッチの約１／２ずれており、奇数行に対し、偶数行の光電変換素子は各行内のピッチの約１／２ずれている多数個の光電変換素子と、対応する光電変換素子列に近接して半導体基板上に形成された帯状平面形状を有し、蛇行しつつ列方向に延在する複数の転送チャネル領域と、転送チャネル領域上方を横断し、全体として行方向に延在し、転送チャネル領域上に複数の区画線を画定する端部重ね合わせ構成を有し、各転送チャネル領域内に区画線で仕切られた複数の電荷転送区画を画定する複数の転送電極とを有し、各転送チャネル領域内で、行方向に沿って、複数の電荷転送区画が並存する領域を含む。



の比は１：１から１：５の間にある請求項１１から２０のいずれか１項に記載の固体撮像装置。

【請求項２２】　２次元表面を画定する半導体基板と、前記半導体基板の表面に一定のピッチで複数列、複数行に配列された多数個の光電変換素子であって、奇数列の光電変換素子に対し、偶数列の光電変換素子は各列内の光電変換素子ピッチの約１／２ずれており、奇数行の光電変換素子に対し、偶数行の光電変換素子は各行内の光電変換素子ピッチの約１／２ずれており、前記各光電変換素子列は、奇数列または偶数列の光電変換素子のみを含む多数個の光電変換素子と、各々が、対応する光電変換素子列に近接して半導体基板上に形成され、１対の側縁で画定された帯状平面形状を有し、蛇行しつつ列方向に延在する複数の転送チャネル領域と、前記転送チャネル領域上方を横断し、全体として行方向に延在する複数の転送電極であって、前記転送チャネル領域上に複数の区画線を画定する端部重ね合わせ構成を有し、各前記転送チャネル領域内に前記区画線で仕切られた複数の電荷転送区画を画定する複数の転送電極とを有し、各前記転送チャネル領域内の前記光電変換素子に近接した位置で、前記行方向に沿って、複数の前記電荷転送区画が並存する領域を含む固体撮像装置を駆動する駆動方法であって、

（ａ）前記光電変換素子に電荷を蓄積する工程と、

（ｂ）前記光電変換素子に隣接する第１電荷転送区画に読出しレベルの電圧を印加するとともに、その行方向に隣接する第２電荷転送区画に転送用のハイレベルの電圧を印加する工程と（ｃ）前記第１電荷転送区画の電圧を転送用ハイレベルに変化させる工程とを含む固体撮像装置の駆動方法。

【請求項２３】　前記工程（ｂ）、（ｃ）が奇数行の光電変換素子と偶数行の光電変換素子に対して繰り返し行なわれる請求項２２記載の固体撮像装置の駆動方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、電荷転送路とそれを用いた固体撮像装置に関し、特に転送性能を改善した電荷転送路とそれを用いた固体撮像装置に関する。

【０００２】なお、本明細書において、転送性能とは転送速度、転送効率を含む概念を示す。

【０００３】

【従来の技術】第１導電型の半導体領域表面に、第２導電型の延在する転送チャネル領域を形成し、この転送チャネル領域表面に絶縁膜を介して複数の転送電極を形成することにより、電荷転送路を形成することができる。転送電極は転送チャネル領域と容量結合し、その電圧を制御することにより転送チャネル領域のポテンシャルを制御することができる。連続的に電荷を転送するためには、転送チャネル領域表面上に複数の転送電極の各端部をオーバーラップさせて形成する。

【０００４】このような電荷転送路を用いた半導体装置として、固体撮像装置が知られている。固体撮像装置は、受光領域中に行列状に配置された光電変換素子と、各光電変換素子列に近接して形成された電荷転送路とを有する。光電変換素子に蓄積された電荷を、電荷転送路に読出し、電荷転送路を転送することにより、画素情報を表す電荷を外部に取り出すことができる。

【０００５】通常、光電変換素子を正方行列状に配置し、電荷転送路を光電変換素子列に近接させ、列方向に直線状に形成する。電荷転送路のポテンシャルを制御する転送電極は、行方向に延在し、各光電変換素子上で切り欠かれた形状を有する。

【０００６】特願平８－２８８８５６号は、列方向、行方向に約１／２ピッチの画素ずらしを採用した固体撮像装置を提案している。各列内で画素である光電変換素子は一定のピッチで配置され、各行内においても光電変換素子は一定のピッチで配列されている。

【０００７】奇数列の光電変換素子に対し、偶数列の光電変換素子は列内のピッチの約１／２ずれた位置に配置されている。又、奇数行の光電変換素子に対し、偶数行の光電変換素子は行内のピッチの約１／２ずれた位置に配置されている。

【０００８】図１１にこの固体撮像装置の構成を概略的に示す。多数の画素（光電変換素子）ＰＩＸは行列状に配置され、列方向にはピッチP_Vで配置され、行方向にはピッチP_Hで配置されている。隣接する列の光電変換素子は、列方向に約（１／２）P_Vずれた位置に配置され、隣接する行の光電変換素子は、行方向に約（１／２）P_Hずれた位置に配置されている。

【０００９】なお、各画素ＰＩＸの上には色フィルターが設けられ、カラー固体撮像装置を構成している。各画素のカラーをＧ(緑色)、Ｂ（青色）、Ｒ(赤色)で示している。チャネルストップ領域ＣＳが、画素ＰＩＸの一方の側辺を取り囲みつつ、列方向に延在して配置され、各列を電気的に分離している。チャネルストップ領域ＣＳと、画素ＰＩＸに挟まれた領域内に垂直電荷転送チャネルが形成される。

【００１０】半導体基板表面に酸化シリコン膜を介して形成される第１ポリシリコン膜と第２ポリシリコン膜により、図中横方向に延在する電荷転送電極Ｅ１、Ｅ２が形成されている。第１ポリシリコン膜表面も酸化シリコン膜で覆われ、第２ポリシリコン膜から絶縁される。

【００１１】電荷転送電極は、各行当り２本形成されている。なお、図示の構成において、各列内における画素ＰＩＸは、２行当り１個形成されているため、各列内において画素１個当り４つの転送電極が形成されている。これら１画素当り４本の電極を４相駆動することにより、各画素から読み出した電荷を独立して垂直方向に転送することができる。

【００１２】電荷転送電極は、電荷転送路内の電荷を列

る。遮光膜上には、さらに平坦化機能を有する平坦化膜が形成され、その上にマイクロレンズが形成される。固体撮像装置の一般的構造に関しては、例えば、特開昭６１－２５２２４号公報の実施例の欄を参照することができる。

【００２９】図１に示すように、その上に積層転送電極を形成した転送チャネル領域５は、転送電極によって複数の区画に仕切られる。これらの区画は、第１層の転送電極１１の境界線６によって画定される。

【００３０】図４（Ａ）は、転送チャネル領域５内の各区画を示す概略平面図である。転送チャネル領域５は、その上方に形成される第１層及び第２層の転送電極１１、１２により、区画Ｓ１、Ｓ２、Ｓ３、Ｓ４に仕切られる。これらの４つの区画Ｓ１～Ｓ４は、列方向に繰り返し配置される。

【００３１】区画Ｓ１の上には、第２ポリシリコン電極１２が配置されている。区画Ｓ２の上には、第１ポリシリコン電極１１が配置されている。区画Ｓ３、Ｓ４の上には、同様第２ポリシリコン電極１２、第１ポリシリコン電極１１が配置されている。なお、奇数列の転送路と偶数列の転送路は、列方向ピッチの約１／２ずれた形状を有する。

【００３２】図４（Ａ）に示す配置において、各区画は、幅の狭い幅狭部と幅の広い幅広部とを有する。隣接する区画Ｓ１、Ｓ２は長い直線状斜辺とその両端に接続された短い水平方向の辺を有する境界線６ａを介して接している。

【００３３】該斜辺は転送チャネル領域の側縁と平行に配置され、転送チャネル領域を行方向に並んだ２つの幅狭部に分離する。各幅狭部は一定幅を有する。一定幅の領域は均一なナローチャネル効果を有する。なお、斜辺は厳密に転送チャネル領域の側縁と平行である必要はなく、実質的に平行であればよい。並存する幅狭部の両側にそれぞれ幅広部が連続している。

【００３４】区画Ｓ２とＳ３の各幅広部は、水平方向の境界線６ｂを介して接している。幅広部はナローチャネル効果の影響が少なく、低いポテンシャルを有する。

【００３５】図４（Ｂ）は、ナローチャネル効果を概略的に説明するための断面図である。ｐ⁻型領域１７中にｎ型領域１８が形成されている。ｐ⁻領域１７とｎ型領域１８間の作り付け電位および印加電圧により、両者の間のｐｎ接合周辺に空乏層が発達する。破線１９は、このような状態における１つの等電位面を概略的に示す。ｎ型領域１８の幅が狭い場合、両側から発達する空乏層が接し、中間領域の底部のポテンシャルも持ち上げてしまう。等電位面１９は幅方向に縮小するのみでなく、深さ方向も縮小する。このように、幅の狭い半導体領域においては、ナローチャネル効果によりポテンシャルが上昇する。

【００３６】電荷転送路の幅が狭くなると、ナローチャネル効果を避けることは難しくなる。電荷転送路の幅が変化すると、電荷転送路内にポテンシャル分布が生じ、円滑に電荷を転送することが困難になり得る。電荷転送路は、例えば、作り付け電位のみにより、ｎ型領域が完全に空乏化する条件に設定される。

【００３７】図４（Ａ）に示す電荷転送路５においては、各区画が幅の広い幅広部と幅の狭い幅狭部とを有する。幅狭部の幅が一定のため幅狭部のナローチャネル効果は均一である。幅の広い幅広部は、幅の狭い幅狭部に比べナローチャネル効果を受ける割合が少なく、幅広部分のポテンシャルは幅狭部よりもが低くなる。従って、電荷は幅狭部分よりも幅広部分に優先的に蓄積される。

【００３８】区画Ｓ４から区画Ｓ１に電荷を転送する場合、区画Ｓ４における電荷は幅広部分に優先的に分布する。区画Ｓ１のポテンシャルを下げると、区画Ｓ４の幅広部分に蓄積された電荷は速やかに区画Ｓ１の幅広部分に転送される。このため、区画Ｓ４から区画Ｓ１に電荷を転送する転送性能を向上することができる。

【００３９】区画Ｓ１と区画Ｓ２は、長い境界線６ａにより接している。区画Ｓ１から区画Ｓ２に電荷を転送する場合、区画Ｓ２のポテンシャルを下げると、長い境界線６ａを横断して、電荷が転送される。すなわち、境界線６ａを横断する電荷転送は、電荷転送路５の長さ方向に生じるのではなく、長い境界線６ａを横断するように生じる。転送領域の断面積が広いため、境界線６ａを介する電荷転送の転送性能は向上する。

【００４０】このようにして、図１に示す積層転送電極構造を有する電荷転送路は、蛇行形状を有するにもかかわらず、高い転送性能を実現することが期待される。実際に転送性能を測定したところ、良好な転送性能を確認することが出来た。

【００４１】図５は、転送電極に対する駆動回路の接続法を示す。駆動回路としては４相駆動回路を用いる場合を示す。第２層転送電極１２ａに、第１相駆動電源φ１が接続され、第１層転送電極１１ａに第２相駆動電源φ２が接続される。同様、第２層転送電極１２ｂ、第１層転送電極１１ｂに第３相駆動電源φ３、第４相駆動電源φ４が接続される。

【００４２】図６は、４相駆動信号を用いた固体撮像素子の駆動方法を説明するための信号波形を示すタイミングチャートである。駆動信号は、転送用ハイレベルＨ、転送用ローレベルＬ及び転送用ハイレベルよりさらに高い読出しレベルＲを有する。読出しレベルＲは例えば＋１５Ｖであり、電荷蓄積領域からｐ⁻型領域２を介して隣接する電荷転送路５に電荷を読み出すことができる。転送用ハイレベルＨは、例えば接地電位であり、転送用ローレベルＬは、例えば－８Ｖである。

【００４３】以下、第２層転送電極１２に読出しレベルの信号を印加する場合を説明する。ｐ－型領域２の内第２層転送電極１２の下に配置される部分が読出しゲート

とができる。また、固体撮像装置の実施例を説明したが、上述の電荷転送路は固体撮像装置に限らず、広く電荷転送路に利用することができる。

【００６１】図１０は、直線状電荷転送路の実施例における、区画形状の例を示す。

【００６２】図１０（Ａ）は、直線状の電荷転送路５が４つの区画Ｓ１、Ｓ２、Ｓ３、Ｓ４の繰り返しにより形成されている場合を示す。各区画Ｓ１～Ｓ４は、図４（Ａ）に示す区画Ｓ１～Ｓ４と同様、幅広部分と幅狭部分を有する。このような構成により、幅広部分による電荷蓄積機能および長い境界線６ａを介した効率な電荷転送が行なえることは図４（Ａ）の電荷転送と同様である。

【００６３】図１０（Ｂ）は、図１０（Ａ）の構成における境界線６ａ、６ｂの水平方向部分を斜めに傾けた構造である。その他の部分は図１０（Ａ）と同様である。境界線６ｂも斜めに傾けたことにより、その長さが長くなり、転送性能が向上する。境界線は、電荷転送路の側縁に対して傾いているが、電荷転送は境界線に対して直交方向に生じ、上述のように効率的な転送が可能である。

【００６４】図１０（Ｃ）は、電荷転送路５を一様に斜めに配置された直線状の境界線６で仕切ることにより、同一形状の区画Ｓを構成した場合を示す。境界線６が水平方向から傾くことにより、その長さが長くなり、転送性能が向上する。

【００６５】図１０（Ｄ）は、境界線６を上向きのシェブロンパターンとした場合を示す。境界線６の長さが長くなり、隣接する区画間の転送性能が向上する。

【００６６】なお、境界線を水平方向または行方向に対して傾ける場合、傾けた効果を明確にするためには、その角度は５度以上とすることが望ましい。電荷転送路中の区画がほぼ同一面積を有する場合を説明したが、区画の面積は必ずしも一定でなくてもよい。但し、効率的な電荷転送を行なうためには、各区画の面積に余り大きな差は付けないことが好ましい。例えば、同一電荷転送路中の任意の２つの区画の面積の比は、１：１から１：５（または５：１）の範囲内とすることが好ましい。

【００６７】２層転送電極の場合を説明したが、３層以上の転送電極で電荷転送路を構成することもできる。また、駆動方式は４相駆動に限らない。

【００６８】以上実施例に沿って本発明を説明したが、本発明はこれらに制限されるものではない。例えば種々の変更、改良、組み合わせが可能なことは当業者に自明であろう。

【００６９】

【発明の効果】以上説明したように、本発明によれば、電荷転送路の転送性能を向上することができる。

【００７０】蛇行する電荷転送路の場合も高い転送性能を実現することにより、直線状の電荷転送路に劣らない転送性能を実現することができる。

【００７１】画素ずらし配置を有する固体撮像装置においては、電荷転送路を蛇行させることが望まれるが、電荷転送路を蛇行させることによる問題点を解決することができる。

【図面の簡単な説明】

【図１】　本発明の第１の実施例を示す概略平面図である。

【図２】　第１の実施例における基板内の不純物添加領域の平面形状を概略的に示す線図及び基板断面図である。

【図３】　第１の実施例における２層転送電極の形状を示す平面図及び基板垂直方向の断面図である。

【図４】　第１の実施例における電荷転送チャネルの区画形状を示す線図及びナローチャネル効果を説明するための概略断面図である。

【図５】　第１の実施例における駆動回路の接続を示す概略平面図である。

【図６】　第１の実施例による固体撮像装置の駆動方法を概略的に示すタイミングチャートである。

【図７】　第１の実施例の変形例を示す平面図である。

【図８】　本発明の第２の実施例による固体撮像装置の構成を概略的に示す平面図である。

【図９】　本発明の第３の実施例による固体撮像装置の構成を概略的に示す平面図である。

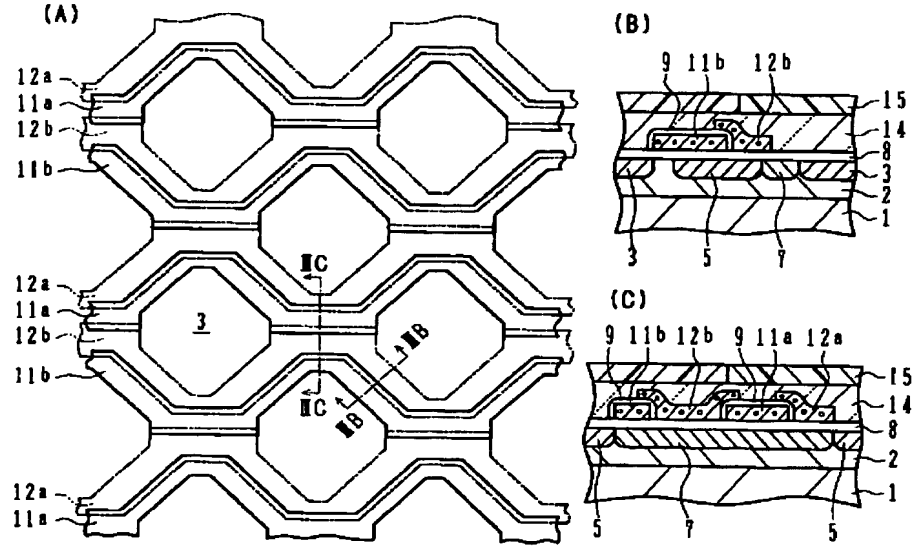
【図１０】　本発明の他の実施例による電荷転送路を示す概略平面図である。

【図１１】　本発明者の先の提案による固体撮像装置の構成を概略的に示す平面図である。

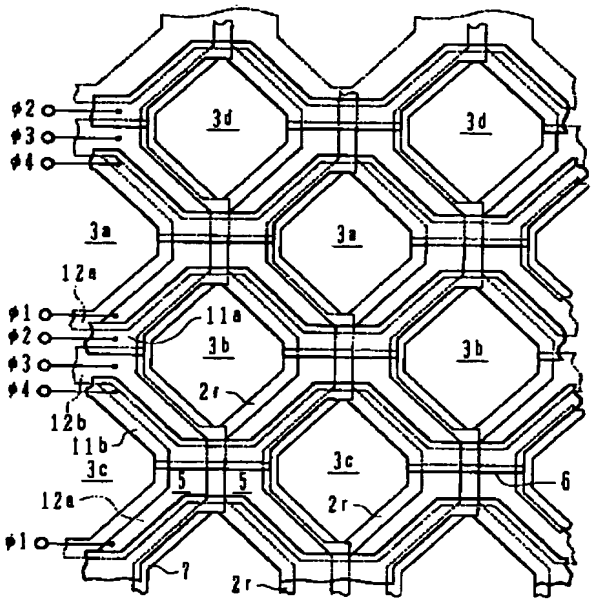
【符号の説明】

１　　ｎ型半導体基板
２　　ｐ型ウエル
３，５　　ｎ型領域
６　　境界線
７　　p^+型チャネルストップ領域
８，９　　酸化シリコン膜
１１，１２　　ポリシリコン転送電極
１４　　絶縁層
１５　　カラーフィルタ層

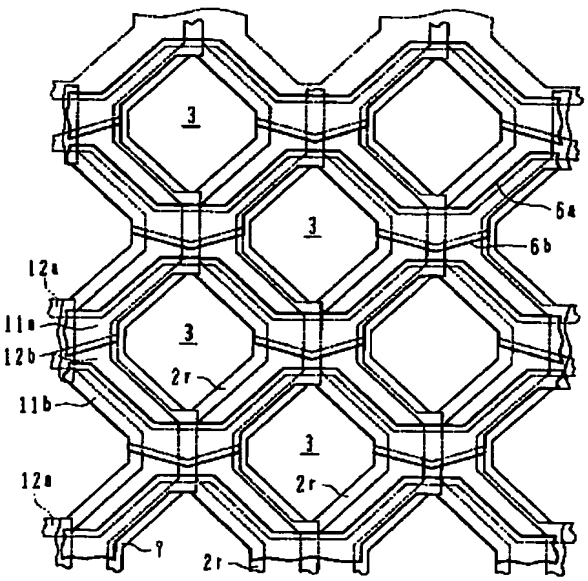
【図３】


(A)
12a
11a
12b
11b
3
ⅡC
ⅡB
(B)
9 11b 12b
15
14
8
3
2
1
(C)
9 11b 12b 9 11a 12a
15
14
8
2
1
5 7 5

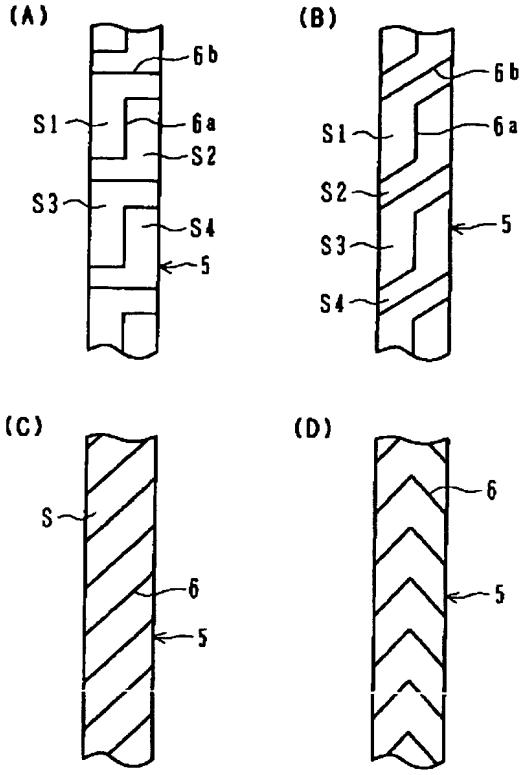
【図５】


φ2
φ3
φ4
3d
3a
12a
φ1
11a
3b
2r
12b
11b
3c
5
6
7

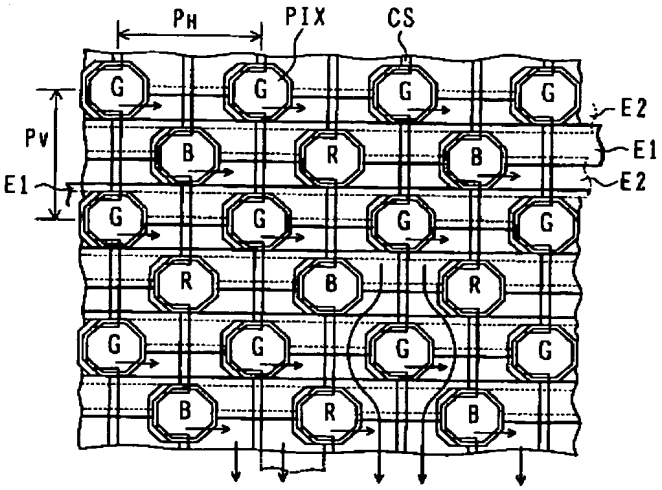
【図７】


3
6a
6b
12a
11a
12b
2r
11b
7

【図１０】



【図１１】



【手続補正書】
【提出日】平成１１年１２月１５日（１９９９．１２．１５）
【手続補正１】
【補正対象書類名】図面
【補正対象項目名】図８
【補正方法】変更
【補正内容】
【図８】